REMARKS

Claims 1, 3, 5-12, 14-15, 17-18, 20 and 24-31 are pending in the application.

Claims 1, 3, 5-12, 14-15, 17-18, 20 and 24-31 are rejected.

Claims 1 and 24-28 stand rejected under 35 U.S.C. 103(a).

Claims 3, 5-12, 14-15, 17-18, 20 and 29-31 stand rejected under 35 U.S.C. 103(a).

Claim 3 has been amended.

Claims 28-31 have been cancelled.

Claims 32-35 have been added.

No new subject matter has been added.

The Applicant respectfully requests reconsideration of claims 1, 3, 5-12, 14-15, 17-18, 20, 24-27, and 32-35.

Specification

The paragraph at page 2, line 21, included a grammatical error where one clause of an "if-then" statement was not in sentence form. The grammatical error was corrected. With respect to the paragraph beginning at page 4, line 19, a space was added between the "21" and the word "also." The remaining paragraphs as set forth now include the words "an embodiment of" prior to the words "the present invention." The Applicant respectfully requests the amendments be entered.

Claim Rejections – 35 USC § 103

Claims 1 and 24-28 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Deering et al. (U.S. Patent No. 5,544,306), hereinafter "Deering."

Claims 3, 5-12, 14-15, 17-18, 20 and 29-31 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Deering et al. in view of Dowdell (U.S. Patent No. 5,301,263), hereinafter "Dowdell."

The Applicant respectfully traverses the rejections.

Claim 1 sets forth "A memory device for use with a memory controller, the memory device comprising: a memory cell array adapted to store internal depth data of an object; a compare circuit; a line connecting the compare circuit to the memory cell array; and a data modifying circuit distinct from the memory controller, the data modifying circuit including the compare circuit and being adapted to: receive corresponding new external depth data of the

object from the memory controller, compare the new external depth data with the internal depth data, transfer the external depth data, via the connecting line, into the memory cell array, depending on the result of the comparison, if the external depth data is transferred, over-write the internal depth data in the memory cell array with the transferred external depth data, and output to the memory controller a status signal."

On the one hand, the Examiner suggests that the new external depth data of claim 1 is the new data N[31..0] of Deering (*see* Office Action, page 3, line 5, *citing* Deering, column 16, lines 62-67). On the other hand, the Examiner suggests that the new external depth data of claim 1 is the write port data 202 (*see* Office Action, page 3, lines 13-15, *citing* Deering, column 17, lines 1-10, which states in part "[t]he pixel buffer write enable signal 276 enables writing of the write port data 202 into the pixel buffer 56."). In either case, Deering fails to teach each limitation of claim 1. And modifying the Deering circuit, as the Examiner suggests, such that connecting line 202 is combined with connecting line 204 to form a single bidirectional line connecting Pixel ALU 235 to pixel buffer 56 does not remedy the failure of Deering to teach each of the elements of claim 1. These points will now be explained in detail.

I. Deering fails to teach each element of claim 1, even if the Deering circuit is modified

A. New data N[31..0] as the "new external depth data" and write port 202 as the "connecting line"

The Examiner suggests that the new external depth data of claim 1 is the new data N[31..0] of Deering (*see* Office Action, page 3, line 5, *citing* Deering, column 16, lines 62-67). But if the new data N[31..0] of Deering is the new external depth data of claim 1 and the write port 202 is the connecting line of claim 1, then the new external depth data is not transferred "via the connecting line, into the memory cell array," as set forth in claim 1. The new data N[31..0] stops at the Pixel ALU 58. Using the close-up view of the Pixel ALU 58 of Figure 8, one can see that the new data N[31..0] is fed into four ROP Blend Units 230-233 and a Compare Unit 235, and then goes no further. The signal carried on the output write port 202 is a blend of internal pixel values, new external pixel values, and other information (*see* Deering, column 6, lines 31-34). The signal carried on the write port 202 is not the new data N[31..0]. As such, even though the write port 202 ("connecting line") connects the Pixel ALU 58 ("memory device") to the pixel buffer 56 ("memory cell array"), the new data N[31..0] ("new external depth data") is not transferred via the write port 202 ("connecting line") into the pixel buffer 56

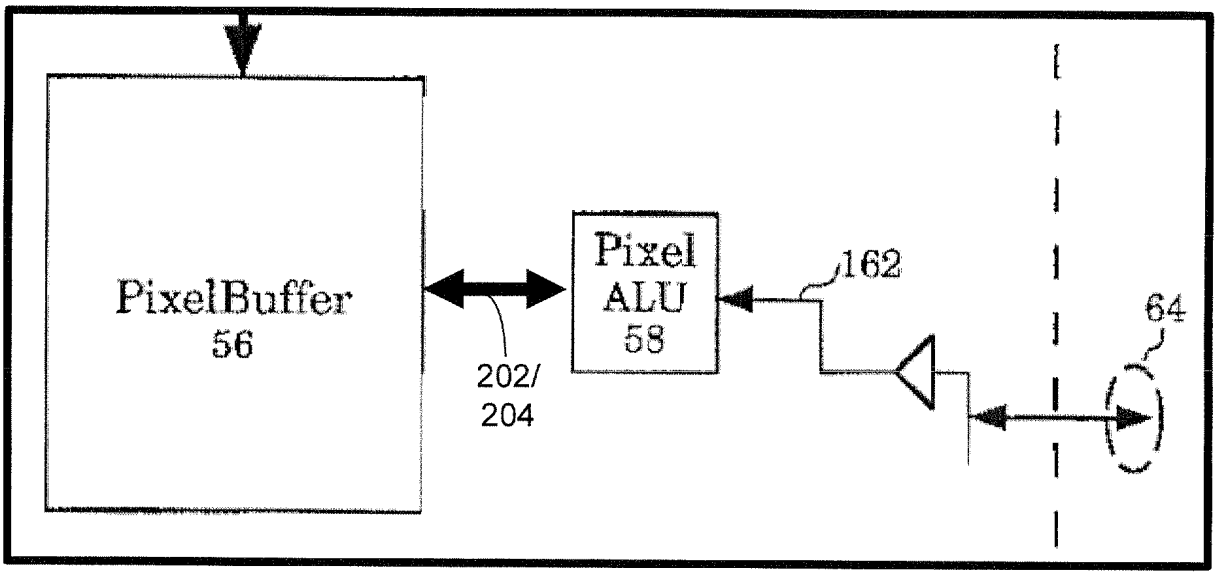
("memory cell array"). Thus, such an interpretation fails to show how each element of claim 1 is taught.

B. New data N[31..0] as the "new external depth data" and read port 204 as the "connecting line"

If the new data N[31..0] of Deering is the new external depth data of claim 1 and the read port 204 is the connecting line of claim 1, then the new external depth data is not transferred "via the connecting line, into the memory cell array," as set forth in claim 1. "The read port data 204 from the pixel buffer 56 provides old data (O[31..0]) for raster operations, blend operations and compare operations" (*see* Deering, column 15, lines 24-26). Thus, the read port data 204 provides old data O[31..0] ("internal depth data") from the pixel buffer 56 ("memory cell array") to the Pixel ALU 58 ("memory device"), and does not transfer the new data N[31..0] ("new external depth data") via the read port 204 ("connecting line") into the Pixel Buffer 56 ("memory cell array"). Thus, Deering fails to teach each element of claim 1.

C. New data N[31..0] as the "new external depth data" and write port 202/read port 204 being modified to form a "single bidirectional line"

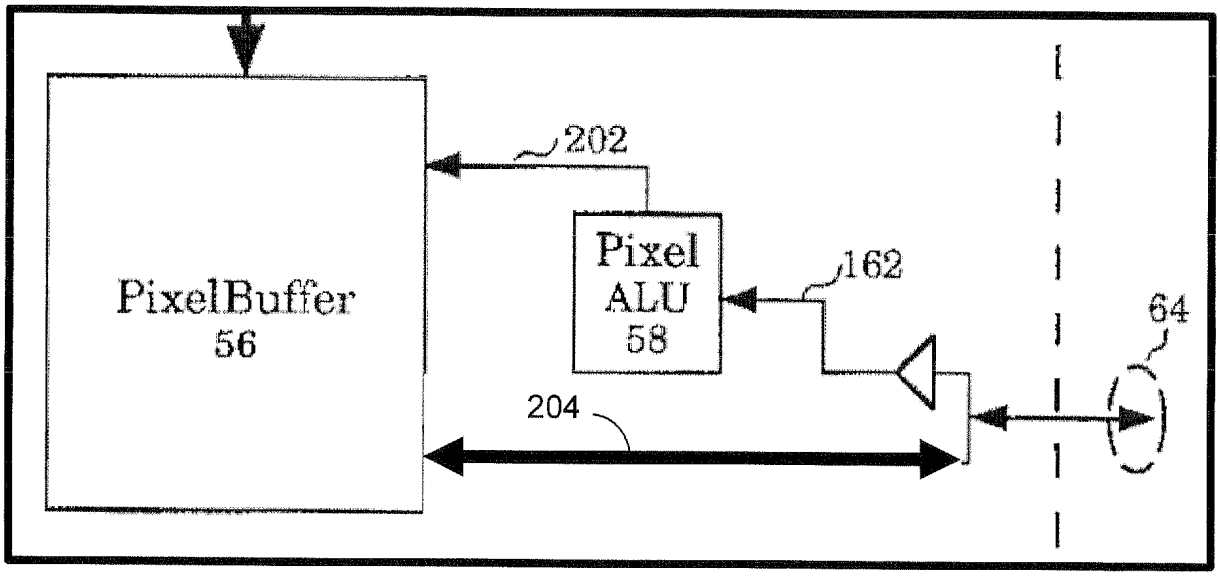
The Examiner states that "Deering can be modified so connecting line 202 is combined with connecting line 204 to form a single bidirectional line connecting compare circuit 235 to memory cell array 56, and so the external depth data can be transferred via this bidirectional line into the memory cell array 56" (*see* Office Action, page 2, section 2). But even if it is well-known in the art to combine the write port 202 with the read port 204, such a bidirectional line would still fail to teach each limitation of claim 1. For example, the Applicant has modified a portion of figure 2 of Deering to show a bidirectional line 202/204, as indicated by the bold double-sided arrow labeled 202/204:



The Applicant submits that even with such a modified circuit, Deering does not teach that the new data N[31..0] ("new external depth data") received on line 162 (*see* Deering, column 15, lines 26-28) is transferred into the Pixel Buffer 56 ("into the memory cell") as set forth in claim 1. The new data N[31..0] must still undergo the blending of internal pixel values, new external pixel values, and other information as a result of the Pixel ALU 58 operations (*see* Deering, column 6, lines 31-34). Thus, the new data N[31..0] again stops at the Pixel ALU 58 ("memory device") and is not transferred "into the memory cell" as set forth in claim 1.

D. New data N[31..0] as the "new external depth data" and read port 202 being modified to form a "single bidirectional line"

Though not suggested by the Examiner, it may be argued that the read port 204 is modified to be a bidirectional line 204, and the write port 202 remains as is. The Applicant has modified a portion of figure 2 of Deering to show a bidirectional line 204, as indicated by the bold double-sided arrow labeled 204:



In this case, the modified circuit of Deering would still fail to teach each limitation of claim 1. For example, if the new data N[31..0] is the new external depth data and the modified read port 204 is the connecting line of claim 1, then the external depth data is not transferred into the Pixel Buffer 56 ("memory cell array") depending on the result of a comparison of the new external depth data with the internal depth data, as set forth in claim 1. Thus, Deering fails to teach each element of claim 1, and claim 1 is in proper form for allowance.

E. Write port data 202 as the "new external depth data"

The Examiner suggests that the new external depth data of claim 1 is the write port data 202 (*see* Office Action, page 3, lines 13-15, *citing* Deering, column 17, lines 1-10, which states in part "[t]he pixel buffer write enable signal 276 enables writing of the write port data 202 into the pixel buffer 56."). But if the write port data 202 is the new external depth data of claim 1, then the new external depth data is not received "from the memory controller" as set forth in claim 1. Rather, the write port data 202 originates internal to the Pixel ALU 58. For example, the Pixel ALU 58 uses four ROP Blend Units 230-233 to combine "one byte of old internal pixel values with one byte of new pixel values and related information received over the rendering bus 98" (*see* Deering, column 6, lines 31-34). The pixel blending equation for each of the ROP Blend units is BLEND RESULT=NEW DATA.times.NEW FRACTION+OLD DATA.times.OLD FRACTION (*see* Deering, column 16, lines 23-25). After applying the pixel blending equation, "[t]he adder 224 generates an intermediate blend result. The intermediate blend result is clamped by the clamp circuit 226. The clamp circuit 226 clamps an adder

underflow to 0 and clamps an adder overflow to 255. The clamped result 348 is transferred via the write port data 202 to the pixel buffer 56 . . . (*see* Deering, column 16, lines 31-36).

Thus, the write port data 202 is not the new external depth data, which is transferred to the memory cell array from the memory controller, and "over-writes[s] the internal depth data in the memory cell array with the transferred external depth data," as set forth in claim 1. And as explained above, even if the read port 204 and the write port 202 are modified to be a bidirectional line, the write port data 202 nonetheless will be a product of the ROP Blend Units 230-233, which blend old internal pixels values, new pixel values, and other information. Therefore, Deering fails to teach each of the limitations of claim 1.

Claims 24-27 depend from claim 1. Based at least on this dependency, and on their own merits, claim 24-27 are likewise in allowable form.

Claim 28 has been cancelled.

II. Deering in view of Dowdell fail to teach each element of claims 3, 5-12, 14-15, 17-18, 20 and 29-31, whether individually or in combination with one another

Claim 3 has been amended to set forth the memory device of claim 1, further comprising " a first control pin for receiving a first control signal originally from the memory controller; and a control circuit for transmitting the external depth data to the memory cell array thereby bypassing the data modifying circuit depending on a state of the first control signal."

With respect to claim 3, the Examiner suggests that the PA_PASS_IN signal is the control pin for receiving a first control signal. The Examiner acknowledges that Deering does not teach bypassing the data modifying circuit depending on a state of the first control signal (*see* Office Action, page 6). Further, it is suggested that the INVALID bit of Dowdell ("The value of the INVALID bit for a particular pixel indicates whether or not the corresponding z-value memory location has a valid z-value stored in it" *see* Dowdell, column 4, lines 5-8) is the first control signal. However, if the INVALID bit is the first control signal, then the first control signal is not received originally from the memory controller, as set forth in claim 3. Rather, the INVALID bit ("first control signal") is received originally from memory (*see, e.g.,* Dowdell, column 4, lines 15-21). Thus, Deering, even if combined with Dowdell fails to teach each of the limitations of amended claim 3. Thus, claim 3 is allowable.

Claim 5 sets forth the memory device of claim 3, wherein "the status signal is output through the first control pin." After first suggesting that the first control pin is the PA_PASS_IN signal (*see* Office Action, page 6, section 12), the Examiner then suggests with respect to claim 5

that the first control pin is the PA_PASS_OUT signal (*see* Office Action, page 7, section 13). It is unclear to the Applicant how the first control pin can be both the PA_PASS_IN signal and the separate PA_PASS_OUT signal. Thus, based at least on its dependency from claim 1, and on its own merits, claim 5 is allowable.

Claims 6-11 depend from claim 1. Based at least on this dependency, and on their own merits, claims 6-11 are allowable.

Claim 12 is in proper form for allowance based at least on similar reasons as set forth above with respect to claim 1.

Claims 14-15 and 17 depend from claim 12. Based at least on this dependency, and on their own merits, claims 14-15 and 17 are allowable.

Claims 18 and 20 are in proper form for allowance based at least on similar reasons as set forth above with respect to claim 5.

Claims 29-31 have been cancelled.

III. New Claims

New claims 32-35 have been added. New claim 32 sets forth "A method for processing depth data of an object in a memory device controlled by a memory controller, the method comprising: generating at least seven clock cycles; receiving an activate command from the memory controller responsive to a first of the at least seven clock cycles; receiving a depth-compare write command from the memory controller responsive to a third of the at least seven clock cycles; receiving external depth data responsive to the third of the at least seven clock cycles, the external depth data indicating a distance between the object on a display screen and a viewer; receiving at least one control signal from the memory controller responsive to the third of the at least seven clock cycles; comparing the received external depth data with internal depth data stored in a memory cell array of the memory device, the comparing being completed before one of a sixth and a seventh of the seven clock cycles."

One of the problems of the prior art with is that a single read-modify-write operation requires ten (10) clock cycles to complete. Using embodiments of the present application, only six (6) or seven (7) clock cycles are sufficient for performing one read-modify-write operation, and performance is increased by more than 30% compared with the prior art (*see* Specification, page 8, lines 7-11). The Applicant submits that the prior art fails to teach each of the elements of claim 32; thus, claim 32 is allowable. Claims 33-35 depend from claim 32. Based at least on this dependency, and on their own merits, claims 33-35 are likewise allowable.

VI. Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1, 3, 5-12, 14-15, 17-18, 20, 24-27, and 32-35 of the application as amended is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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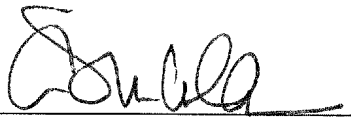

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